What Is Claimed Is:

1. A matrix form semiconductor package substrate having an electrode situated in-between a plurality of integrated circuit (IC) package substrates for providing electrical communication to conductive pads situated on the substrate comprising:

a plurality of IC package substrates integrally formed on a substrate strip in a matrix form having a boundary between each two of said plurality of IC package substrates, each of said plurality of IC package substrates having a multiplicity of conductive pads; and

an electrode formed in a serpentine configuration along said boundary for providing electrical communication to said multiplicity of conductive pads and for providing insulation between said multiplicity of conductive pads after said plurality of IC packages are cut along said boundary through said electrode.

2. ~~A~~ The matrix form semiconductor package substrate having ~~an~~ said electrode situated in-between ~~a~~ said plurality of integrate circuit (IC) package substrates according to claim 1, wherein said electrode being a plating bar formed of an electrically conductive material.

3. ~~A~~ The matrix form semiconductor package substrate having ~~an~~ said electrode situated in-between ~~a~~ said plurality of integrate circuit (IC) package substrates according to claim 1, wherein said electrode being a plating bus formed of copper.

4. ~~A~~ The matrix form semiconductor package substrate having ~~an~~ said electrode situated in-between ~~a~~ said plurality of integrate circuit (IC) package substrates according to claim 1, wherein said plurality of IC package substrates being at least four IC package substrates arranged in ~~a~~ said matrix form.

5. ~~A~~ The matrix form semiconductor package substrate having ~~an~~ said electrode situated in-between ~~a~~ said plurality of integrate circuit (IC) package substrates according to claim 1, wherein said matrix form semiconductor substrate being for a ball grid array package.

6. ~~A~~ The matrix form semiconductor package substrate having ~~an~~ said electrode situated in-between ~~a~~ said plurality of integrate circuit (IC) package substrates according to claim 1, wherein said plurality of IC package substrates integrally formed in such a way that traces on adjacent package substrates at corresponding opposite positions are connected together by said electrode.

7. ~~A~~ The matrix form semiconductor package substrate having ~~an~~ said electrode situated in-between ~~a~~ said plurality of integrate circuit (IC) package substrates according to claim 1, wherein said multiplicity of conductive pads being connected electrically to a multiplicity of wirebond fingers by a multiplicity of traces.

8. ~~A~~ The matrix form semiconductor package substrate having ~~an~~ said electrode situated in-between ~~a~~ said plurality of integrate circuit (IC) package substrates according to claim 1, wherein said electrode being formed in a corrugated configuration.

9. A matrix form semiconductor package substrate having an electrode situated in-between a plurality of integrate circuit (IC) package substrates according to claim 1, wherein said electrode being formed in a corrugated configuration with each one of two legs of a corrugation connected to an oppositely positioned IC package substrates.

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10. ~~A~~ matrix form semiconductor package substrate having ~~an~~ said electrode situated in-between ~~a~~ said plurality of integrate circuit (IC) package substrates according to claim 1, wherein said electrode provides electrical communication to said multiplicity of conductive pads by electrically connecting to a plating bath.

11. ~~A~~ ball grid array package substrate comprising:

an insulating substrate having a top surface;

a multiplicity of conductive traces emanating from each one of said plurality of BGA package substrates, each of said multiplicity of conductive traces provides electrical communication between a conductive pad and a wirebond finger situated on a BGA package; and

an electrode having a serpentine configuration electrically connected to said multiplicity of conductive traces.

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12. ~~A~~ ball grid array package substrate according to claim 11, wherein said electrode being formed in a corrugated configuration.

13. The ball grid array package substrate according to claim 11, wherein said electrode being formed in a corrugated configuration with each one of two legs of a corrugation connected to a trace of an oppositely positioned BGA package substrate.

14. The ball grid array package substrate according to claim 11, wherein said electrode being a plating bar formed of an electrically conductive metal.

15. The ball grid array package substrate according to claim 11, wherein said electrode being a plating bus being connected to a plating bath in an electroplating process.

16. The ball grid array package substrate according to claim 11 further comprising a plurality of solder balls formed on a bottom surface of said BGA package substrate.

17. The ball grid array package substrate according to claim 11, wherein said serpentine configuration having an amplitude between about 0.3 mm and about 5 mm.

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18. ~~A~~ matrix form semiconductor package substrate having ~~an~~ said electrode situated in-between ~~a~~ said plurality of integrate circuit (IC) package substrates according to claim 1, wherein said serpentine configuration of said electrode having an amplitude between about 0.3 mm and about 5 mm.